In the Claims

Claims 1-42 (canceled).

Claim 43 (currently amended): A method of forming a transistor device, comprising:

forming a gate stack over a semiconductor substrate; the gate stack comprising an electrically insulative pad, at least one electrically conductive material over the pad, and an electrically insulative cap over the at least one electrically conductive material; the gate stack comprising a pair of opposing sidewalls extending at least along the one or more conductive materials and the cap;

forming an electrically insulative material along the sidewalls;

anisotropically etching the electrically insulative material to form sidewall spacers along the sidewalls;

implanting dopant into the substrate proximate the gate stack to form a pair of source/drain diffusion regions gatedly connected to one another through the gate stack; and

depositing a deuterated silicon nitride-containing material over the gate stack and over the sidewall spacers; the deuterated silicon nitride-containing material being deposited from at least one deuterated nitrogen compound and one or more halogenated silicon compounds that do not contain hydrogen isotopes; the deuterated silicon nitride-containing material being a deuterated silicon oxynitride-containing material.

Claim 44 (cancelled).

Claim 45 (original): The method of claim 43 wherein the electrically insulative material formed along the sidewalls and used to form the sidewall spacers is a deuterated silicon nitride-containing material deposited from at least one deuterated nitrogen compound and one or more halogenated silicon compounds that do not contain hydrogen isotopes.

Claim 46 (original): The method of claim 43 wherein the electrically insulative cap is a deuterated silicon nitride-containing material deposited from at least one deuterated nitrogen compound and one or more halogenated silicon compounds that do not contain hydrogen isotopes.

Claim 47 (original): The method of claim 46 wherein the electrically insulative material formed along the sidewalls and used to form the sidewall spacers is a deuterated silicon nitride-containing material deposited from at least one deuterated nitrogen compound and one or more halogenated silicon compounds that do not contain hydrogen isotopes.

Claim 48 (original): The method of claim 43 wherein the depositing is chemical vapor deposition conducted at a pressure of less than or equal to about 5 Torr.

Claim 49 (original): The method of claim 43 wherein the at least one deuterated nitrogen compound is selected from the group consisting of NH_2D, NHD_2, ND_3, and mixtures thereof.

Claim 50 (original): The method of claim 43 wherein the one or more halogenated silicon compounds consist of silicon and chlorine.

Claim 51 (original): The method of claim 50 wherein the one or more halogenated silicon compounds are selected from the group consisting of $SiCl_4$, Si_2Cl_6 and mixtures thereof.

Claim 52 (original): The method of claim 51 wherein the at least one deuterated nitrogen compound is selected from the group consisting of NH_2D, NHD_2, ND_3, and mixtures thereof.

Claim 53 (original): The method of claim 43 wherein the deuterated silicon nitride-containing material consists essentially of silicon nitride.

Claim 54 (original): The method of claim 43 wherein the deuterated silicon nitride-containing material consists of silicon nitride.

Claim 55 (original): The method of claim 43 wherein a passivation anneal is conducted after forming the deuterated silicon nitride-containing material; the passivation anneal comprising heating the substrate to a temperature of from about 350°C to about 450°C for a time of from about 5 minutes to about 2 hours.

Claim 56 (original): The method of claim 43 further comprising incorporating the transistor device into a DRAM cell.

Claim 57 (original): The method of claim 56 further comprising incorporating the DRAM cell into an electronic system.